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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,993	08/04/2003	Jaroslav Hynecck	TI-36483	5016
23494	7590	02/14/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,993	HYNECEK, JAROSLAV	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 1-10 and 18-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>11/06/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. **Claims 1-10 and 18-20** have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 01/03/2005.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed 11/06/2003. A signed copy of Form PTO-1449 is herewith enclosed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claim 11** is rejected under 35 U.S.C. 102(b) as being anticipated by Kato (5,760,430). Kato teaches (title, abstract, cols. 1, col. 2, l. 1-33, col. 4, l. 10- col. 5, l. 43, col. 6, l. 24-58) and Figures 1 and 5; particularly col. 4, l. 29-50) a charge coupled device comprising:

a first clocked gate 16 coupled to a first clocking signal (through transfer clock H ϕ) (col. 4, l. 36-42);

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a field plate 14 adjacent to the first clocked gate, and coupled to a DC bias source 18 (col. 4, l. 29-42: set to $\frac{1}{2}$ of the peak voltage of clock $H\phi$) (cf. col. 4, l. 29-37)); and

a second clocked gate 15 adjacent to the field plate (cf. Figure 1) and coupled to a second clocking signal (through clock $H\phi'$) (cf. col. 4, l. 43-50), the field plate 14 is between the first clocked gate 16 and the second clocked gate 15 (cf. Figures 1 and 5), and the first clocking signal is clocked out of phase with the second clocking signal (cf. col. 4, l. 50-57: note that the delay time (20 ns) of the delay circuit 21 is more than one-half of one clock cycle of clock $H\phi$, said one half of one clock cycle being 35 ns).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. ***Claims 12 and 13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (5,760,430) in view of McNutt (4,857,979). As detailed above, Kato anticipates claim 11. Kato also teaches a well region 24 (cf. col. 6, l. 24-40), but *Kato does not necessarily* teach well regions under clocked gates, nor does Kato necessarily teach a clocked barrier. *However, it would have been obvious* to include said clocked barrier and clocked well in view of McNutt, who, in a patent on an infrared CCD imaging device (title, abstract, col. 1, col. 2, l. 1- col. 2, l. 27 and col. 2, l. 53 – col. 4, l. 50),

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hence closely related to the invention by Kato, teaches the inclusion of a clocked well 58 (cf. col. 4, l. 21) and barrier gate 52 (cf. col. 4, l. 22) to a clocked gate so as to prevent back-flow of charge carriers (cf. col. 4, l. 21-28). *Motivation* to include the teaching by McNutt into the invention by Kato derives from the enhanced control on the motion of collected charges. The teaching can be combined readily by adding the barrier gate and doping the substrate to each clocked gate.

6. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (5,760,430) in view of Hynecek (5,430,481). As detailed above, Kato anticipates claim 11. Kato does not teach the further limitation as defined by claim 14, although Kato does disclose a solid-state imaging apparatus using his CCD device (cf. abstract). *However, it would have been obvious to include* said further limitation in view of *Hynecek*, who, in a patent on a CCD image sensor, - hence analogous art, teaches the incorporation of a charge transfer device into a solid-state imaging apparatus of the frame transfer type (cf. abstract). In particular, Hynecek teaches the incorporation of the CCD device in an imager including a frame transfer image array defined by reference to this patent in Applicant's specification and as depicted in Figure 1 and described in col. 2, l. 25-48), with the following attributes: two phase imaging area 22, single phase frame memory area 24, dual serial registers 26 and 28, charge detection amplifiers 30 and 32, bottom clearing drain 34, and external connections 12. *Motivation* for inclusion of the teaching by Hynecek in the invention by Kato is application of the CCD device component to an imager compatible with both the NTSC standard and requirements for still photography (col. 1, l. 15-35). *Combination* of the teaching in this regard by

Hynecek in the invention by Kato is easily accomplished by replacing the component for moving the charges (pixel area of Figure 4 in Hynecek) by the equivalent component by Kato.

7. **Claims 11, 15, 16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek (6,278,142 B1; made of record in IDS as item AE) in view of Kato (5,760,430).

On claim 11: Hynecek teaches (title, abstract, col. 5, l. 41 – col. 6, l. 50; Figure 6) a charge coupled device comprising: a first clocked gate 202 coupled to a first clocking signal ϕ_1 (col. 5, l. 45-52); a charge multiplication gate 222 adjacent to the first clocked gate, and coupled to a charge-multiplication gate 222 (col. 5, l. 54-64); and a second clocked gate 203 adjacent to the charge multiplication gate and coupled to a second clocking signal ϕ_2 (cf. col. 5, l. 45-54), the charge-multiplication gate is between the first clocked gate and the second clocked gate (cf. Figure 6), and the first clocking signal is clocked out of phase with the second clocking signal (cf. Figure 7, col. 7, l. 6-23).

Hynecek, in his description of his invention, does not teach the limitation that charge multiplication gate 222 is instead to be coupled to a DC source as claimed. However, it would have been obvious to include said further limitation in view of the teaching by Kato, who teach the possibility to reduce the number of required clocks required (cf. abstract) by coupling the equivalent 14 of gate 222 to a DC signal source 18. As evidenced by the required and sufficient relative voltages among the three gates (cf. Figure 7) a DC signal from the charge multiplication clock ϕ_{cm} can easily be accomplished through providing a signal to ϕ_1 during τ_{cm} such that all potential

differences between all three voltages are exactly the same as in Hynecek Figure 7 while ϕ_{cm} is constant, thus yielding the identical relative voltages during both stages τ_{cm} and τ_{tr} . Therefore, the teaching by Kato in this regard can be easily *combined* with said invention by using the clock signal ϕ_1 instead of clock signal ϕ_{cm} to effect potential differences as required during τ_{cm} . *Motivation* to include the teaching by Kato in the invention by Hynecek derives from the resulting decrease in complexity of the clock system through reduction of the number of clocks required.

On claim 15: the device by Hynecek is a Full Frame device, comprising IMPACTRON cell 201 as depicted by Figures 5 and 6 and which is a defining portion of the Full Frame device by Hynecek (6,278,142 B1; IDS AE) (col. 8, l. 65-67).

On claim 16: the device by Hynecek comprises an anti-blooming drain (cf. Figure 15 and col. 14, l. 21-32).

On claim 17: the invention when combined with Kato still is a charge-multiplying device because the field plate replacing charge-multiplication gate 222 still causes charge multiplication since none of the relative voltages is modified by the replacement.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 9, 2005.

Patent Examiner:



Johannes Mondt (Art Unit: 2826).